REMARKS

The claims remaining in the present application are Claims 1-11, 13, and 21-25. Claims 1-3, 5-6, 8-11, 13, and 21 have been amended. Claims 22-25 have been added. No new matter has been added as a result of these claim amendments.

CLAIM REJECTIONS

Claims 1-13 and 21 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Mason et al., U.S. Patent No. 5,946,219 (hereinafter Mason) in view of Varadarajan et al., U.S. Patent No. 5,838,583 (hereinafter Varadarajan). Claim 12 has been cancelled, without prejudice. As a result, the rejection to Claim 12 is moot. The rejection to Claims 1-11, 13, and 21 is respectfully traversed for the reasons below.

CLAIMS 1-7

Claim 1 reads:

> A computer implemented method of generating an order of loading data into a programmable device comprising the steps of:
>
> a) automatically identifying a plurality of configuration bits for programming a programmable device by traversing a hierarchical schematic representation of the programmable device;
>
> b) automatically determining a plurality of addresses corresponding to said plurality of configuration bits, said plurality of addresses being in an address space of a memory of the programmable device and operable to store configuration bits for programming the programmable device;
>
> c) automatically determining a plurality of logical names for said plurality of configuration bits; and
>
> d) based on an order in which said address space is traversed when programming said programmable device, automatically storing said plurality of logical names for said plurality of configuration bits within a data structure within computer readable memory, wherein said data structure describes an order in which to program said programmable device.

Applicants respectfully assert that the combination of Mason and Varadarajan fail to teach or suggest the claimed limitation of, "automatically identifying a plurality of configuration bits for programming a programmable device by traversing a hierarchical schematic representation of the programmable device."

Mason and Varadarajan may disclose techniques that assist the placement and routing stages of design. As an example, Mason discloses that the placement and routing generates a design database comprising resources use in the FPGA (e.g., logic cells, I/O blocks, interconnects). However, Applicants assert that specifying the resources of the FPGA does not involve traversing a hierarchical schematic representation of the programmable device. Thus, Applicants respectfully assert that the placement and design taught in Mason and Varadarajan does not teach or suggest this claimed limitation.

Mason and Varadarajan may disclose a bitstream compiler that generates the configuration bits. However, the bitstream compilers in Mason and Varadarajan do not traverse a hierarchical schematic representation of the programmable device to identify configuration bits, to Applicants understanding. Thus, the bitstream compilers taught in Mason and Varadarajan do not teach or suggest this claimed limitation.

For the foregoing rationale, the combination of Mason and Varadarajan fails to teach or suggest the limitations of Claim 1. Therefore, Applicants respectfully solicit the allowance of Claim 1.

Claims 2-7 and 21 depend from Claim 1, which is believed to be allowable. As such, Claims 2-7 and 21 are respectfully believed to be allowable.

CLAIMS 8-13

Amended Claim 8 reads:

> A computer implemented method of generating an order of loading data into a programmable logic device comprising the steps of:
> a) accessing a data structure comprising a plurality of logical names corresponding to a plurality of addresses in an address space of a memory operable to store configuration bits for programming a programmable logic device;

b) accessing a data structure specifying an order in which said plurality of addresses are traversed when loading said configuration bits into said programmable logic device;

c) automatically ordering said plurality of logical names from step a) based on the order specified in said data structure in step b) and information in the data structure comprising the plurality of logical names corresponding to the plurality of addresses; and

d) automatically storing said ordered plurality of logical names from step c) in a data structure within computer readable memory, wherein said ordered plurality of logical names describe an order of loading said configuration bits into said programmable logic device.

The combination of Mason and Varadarajan fails to teach or suggest "automatically ordering said plurality of logical names from step a) based on the order specified in said data structure in step b) and information in the data structure comprising the plurality of logical names corresponding to the plurality of addresses." Applicants note that the database claimed in a) recites that the addresses are in an address space of a memory operable to store configuration bits for programming a programmable logic device, and that the database in b) specifies the order in which said plurality of addresses are traversed when loading said configuration bits.

Mason and Varadarajan may disclose bitstream compilers. However, the bitstream compilers does not automatically order logical names, to Applicants understanding. Rather, bitstream compilers generate a series of bits. Therefore, the bitstream compilers do not teach or suggest this claimed limitation.

Mason and Varadarajan may also disclose routing and placement techniques, which may create a design database. However, such techniques are not themselves concerned with the addresses in the address space of a memory operable to store configuration bits for programming a programmable logic device. Further, any ordering of resources that is accomplished by placing and/or routing is not based on the order in which said plurality of addresses are traversed when loading said configuration bits.

Therefore, the routing and placement techniques disclosed by Mason and Varadarajan do not teach or suggest the above claim limitation.

For the foregoing rationale, Claim 8 is not rendered obvious over Mason in view of Varadarajan. Therefore, allowance of Claim 8 is respectfully requested.

Claims 9-11 and 13 depend from Claim 8. As Claim 8 is respectfully believed to be allowable, allowance of Claims 9-11 and 13 is respectfully solicited.

CLAIMS 14-20

Claims 14-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mason. The rejection moot in light of the cancellation of Claims 14-20, without prejudice.

NEW CLAIMS

Claims 22-25 have been added. Support for Claim 22 may be found in the instant specification at least at page 29, line 10 - page 32, line 15. Support for Claims 23-25 may be found in the instant specification at least at page 3, lines 14-16 and page 9, line 3 - page 25, line 20. No new matter has been added as a result of these new claims.

Claim 22 recites, in part:

> c) constructing a bit order data structure within computer readable memory that describes an order of loading said configuration bits into said programmable logic device by repeating said c1) - c3) for addresses in the address space based on the address order data structure:
>
> c1) determining whether an address in the address space comprises a configuration bit, based on the configuration bit data structure;
>
> c2) automatically storing a space in said bit order data structure responsive to a determination in said c1) that there is no configuration bit at the address in the address space; and
>
> c3) automatically storing the logical name of the configuration bit in the bit order data structure based on the configuration bit data structure,

responsive to a determination in said c1) that there is a configuration bit at the address in the address space.

Applicants respectfully assert that the cited prior art fails to teach or suggest the above-recited limitations. For example, Applicants respectfully assert that neither the placement and routing techniques nor the bitstream compiler, as disclosed by Mason and Varadarajan teach or suggest, "constructing a bit order data structure within computer readable memory that describes an order of loading said configuration bits into said programmable logic device by repeating said c1) - c3) for addresses in the address space based on the address order data structure," as claimed.

Moreover, Applicants respectfully submit that, "determining whether an address in the address space comprises a configuration bit, based on the configuration bit data structure," is neither taught nor suggested by the prior art for at least reasons already discussed herein.

Moreover, Applicants respectfully submit that, "automatically storing a space in said bit order data structure responsive to a determination in said c1) that there is no configuration bit at the address in the address space," is neither taught nor suggested by the prior art for at least reasons already discussed herein.

Moreover, Applicants respectfully submit that, "automatically storing the logical name of the configuration bit in the bit order data structure based on the configuration bit data structure, responsive to a determination in said c1) that there is a configuration bit at the address in the address space," is neither taught nor suggested by the prior art for at least reasons already discussed herein.

For the foregoing reasons, Applicants respectfully assert that Claim 22 is allowable of the prior art. Claims 23-25 depend from Claim 22. Therefore, Claims 23-25 are respectfully believed to be allowable over the prior art. Consequently, Applicants earnestly request allowance of Claims 22-25.

CONCLUSION

In light of the above listed amendments and remarks, reconsideration of the rejected Claims is requested. Based on the arguments and amendments presented above, it is respectfully submitted that Claims 1-11, 13, and 21-25 overcome the rejections of record. Therefore, allowance of Claims 1-11, 13, and 21-25 is earnestly solicited.

Should the Examiner have a question regarding the instant amendment and remarks, the Applicants invites the Examiner to contact the Applicants' undersigned representative at the below listed telephone number.

Respectfully submitted,
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Dated: 3/22, 2004

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